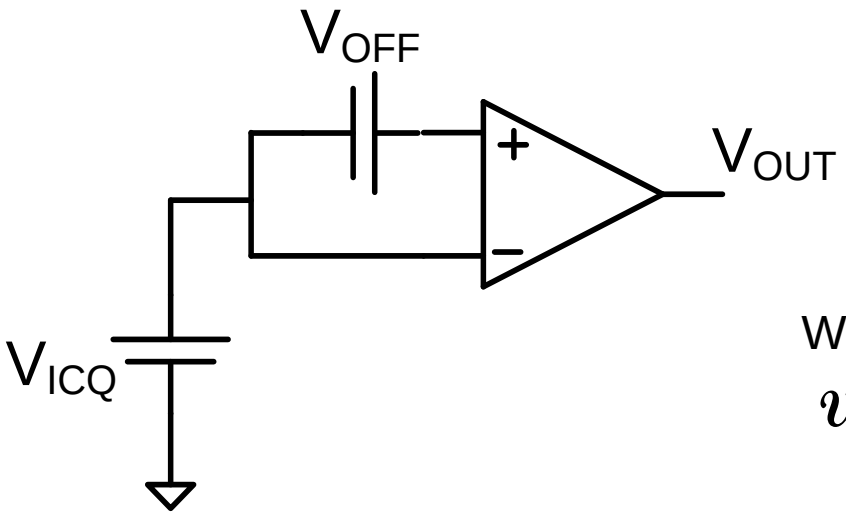
EE 435

Lecture 22

Offset Voltages

Review from last lecture

Offset Voltage



When operating linearly

$$v_{OUT}=A_D v_D+A_C v_C$$

Definition: The input-referred offset voltage is the differential dc input voltage that must be applied to obtain the desired output when V_{ic} is the quiescent common-mode input voltage.

V_{OFF} is usually related to the output offset voltage by the expression

$$V_{OFF}=\frac{V_{OUTOFF}}{A_D}$$

V_{OFF} is dependent upon V_{ICQ} although this dependence is usually quite weak and often not specified

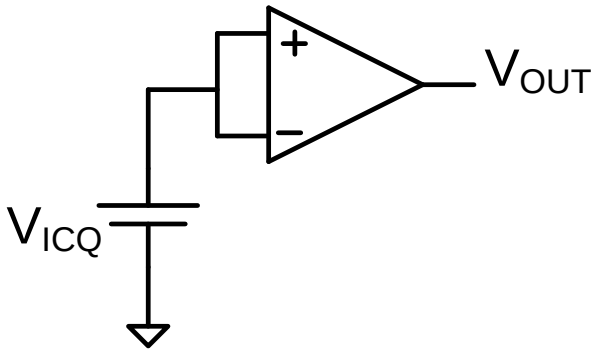
V_{OFF} almost always large enough to force op amp out of linear mode for good op amps if used open loop

Review from last lecture

Offset Voltage

Two types of offset voltage:

- Systematic Offset Voltage
- Random Offset Voltage

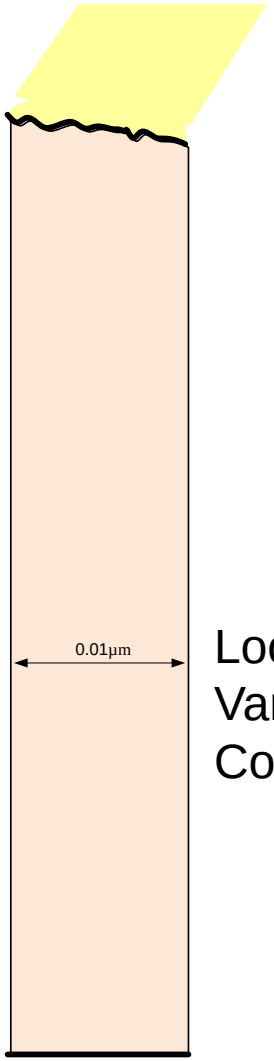


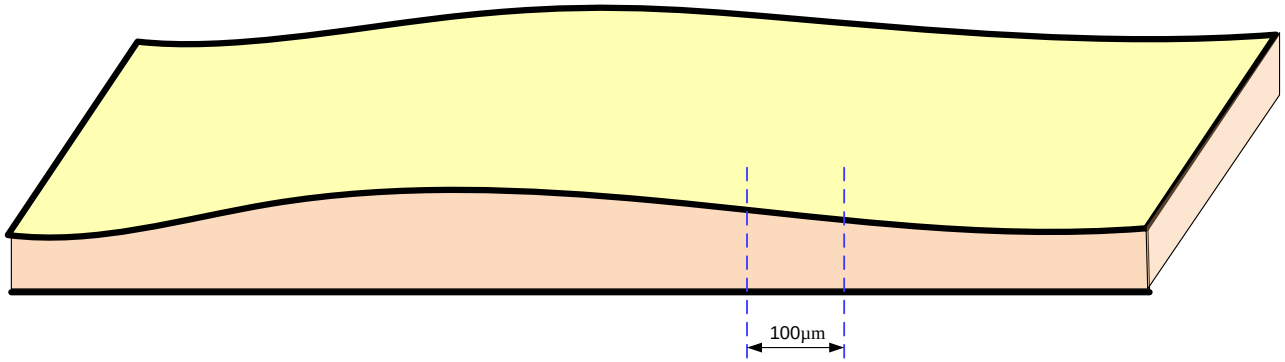
After fabrication it is impossible (difficult) to distinguish between the systematic offset and the random offset in any individual op amp

Measurements of offset voltages for a large number of devices will provide mechanism for identifying systematic offset and statistical characteristics of the random offset voltage

Review from last lecture

Gradient and Local Random Effect





Gradient Effects : Locally Appear Linear

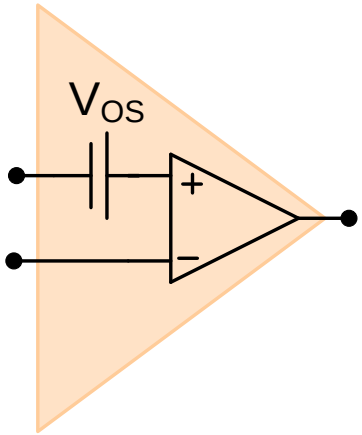
- Magnitude and Direction of Gradients are random
- Highly Correlated over Short Distances

Local Random Effects : Vary Locally With No Correlation

- **Both Contribute to Offset**
- **Both are random variables**
- **If Not Managed, Both Can Cause Large Offsets**
- **Strategies for minimizing their effects are different**
- **Will refer to the local random effects as “random” and the random gradient effects as “gradient” effects**

Review from last lecture

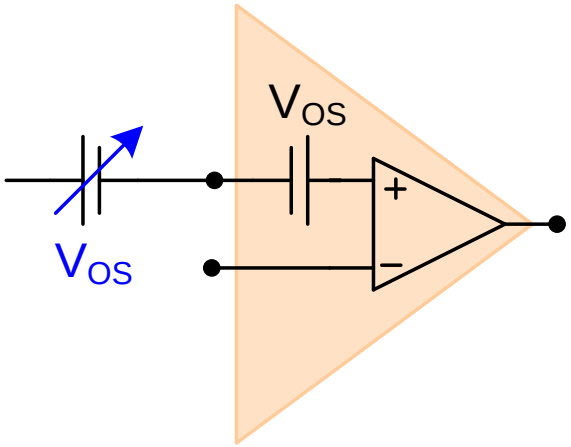
Offset Voltage



Can be modeled as a dc voltage source in series with the input

Review from last lecture

Offset Voltage



Effects can be reduced or eliminated by adding equal amplitude opposite DC signal (many ways to do this)

Widely used in offset-critical applications

Comes at considerable effort and expense for low offset

Prefer to have designer make V_{OS} small in the first place

Review from last lecture

Effects of Offset Voltage

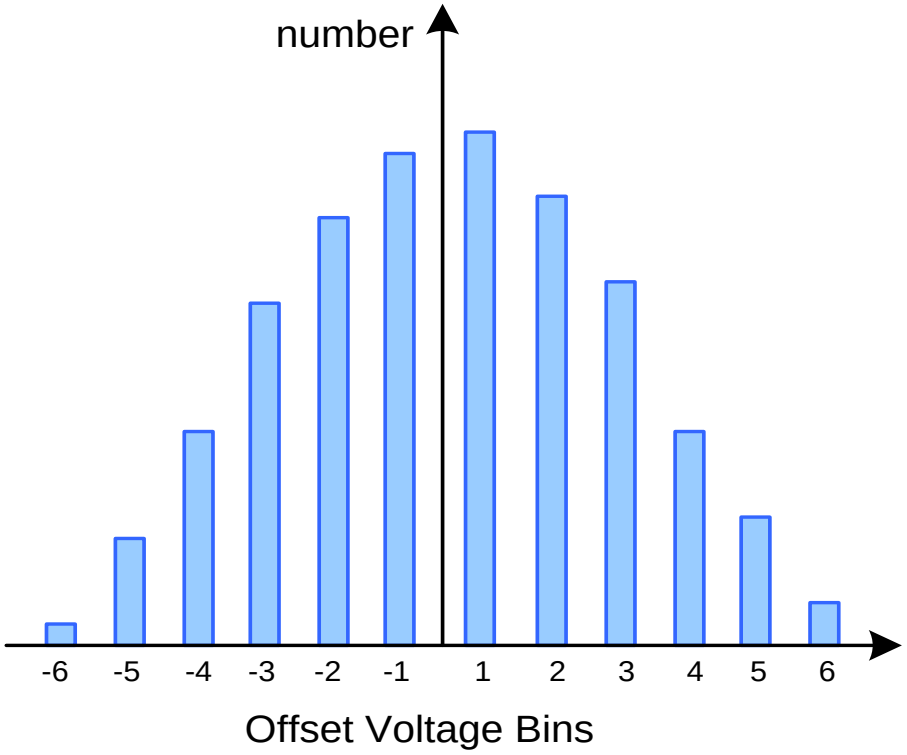
- Deviations in performance will change from one instantiation to another due to the random component of the offset

- Particularly problematic in high-gain circuits

- A major problem in many other applications

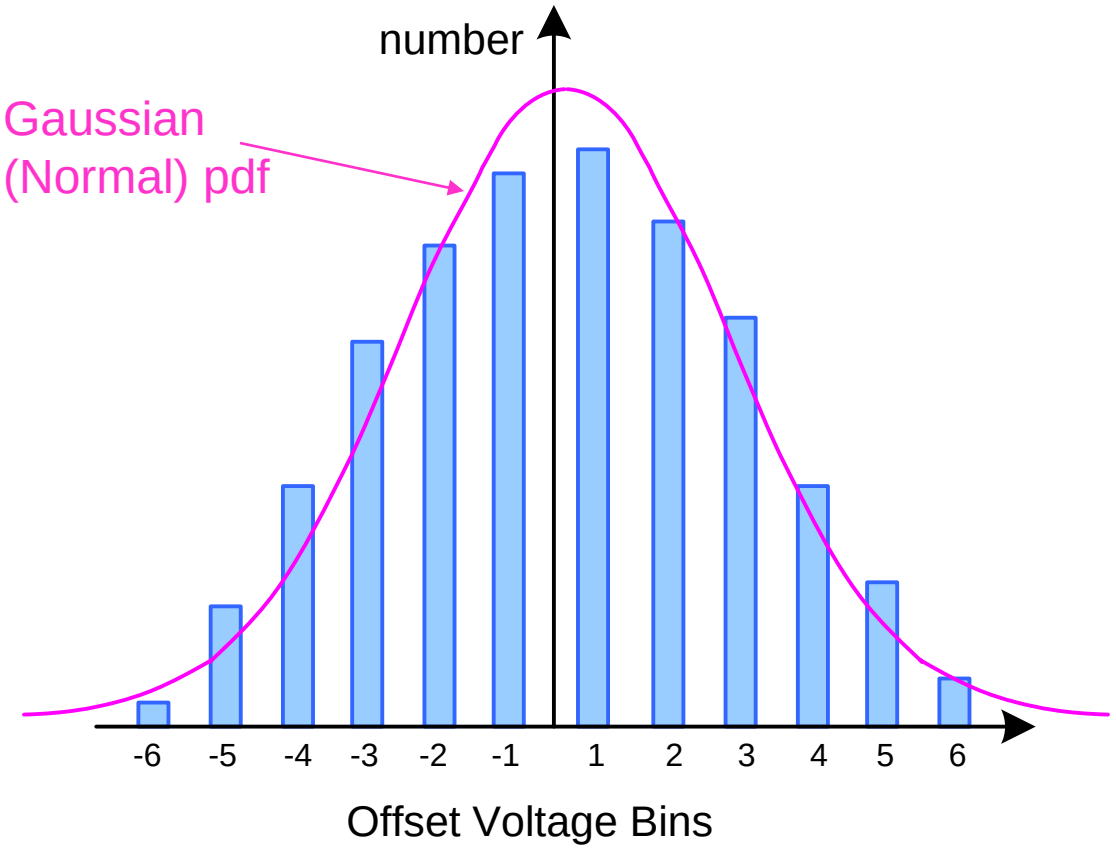
- Not of concern in many applications as well

Offset Voltage Distribution



Typical histogram of random offset voltage (binned) after fabrication

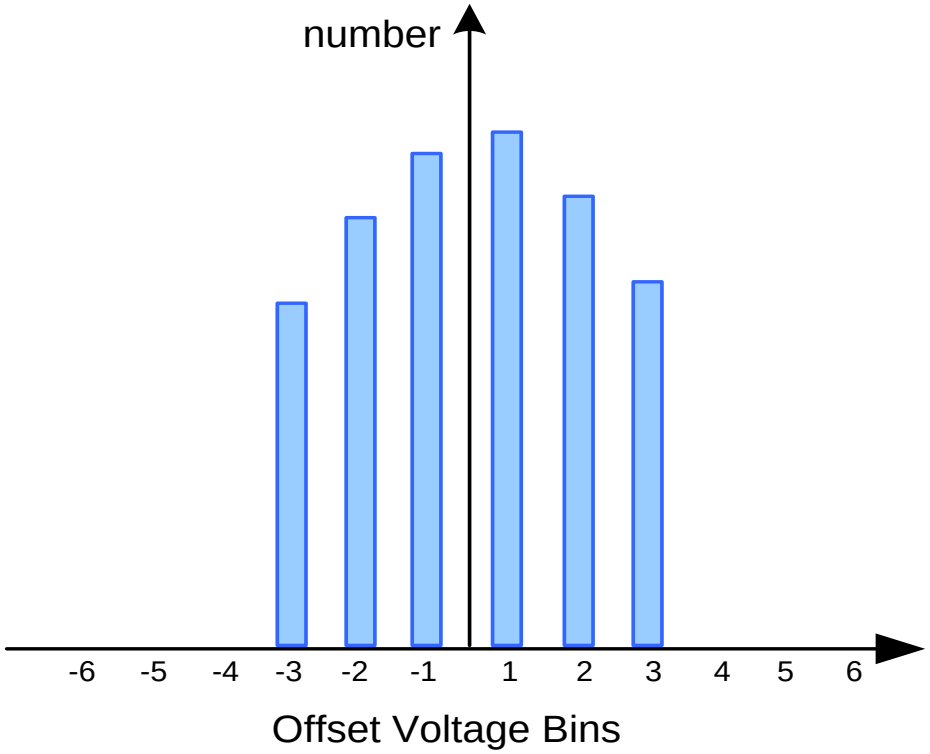
Offset Voltage Distribution



Typical histogram of offset voltage (binned) after fabrication

Mean is nearly 0 (actually the systematic offset voltage)

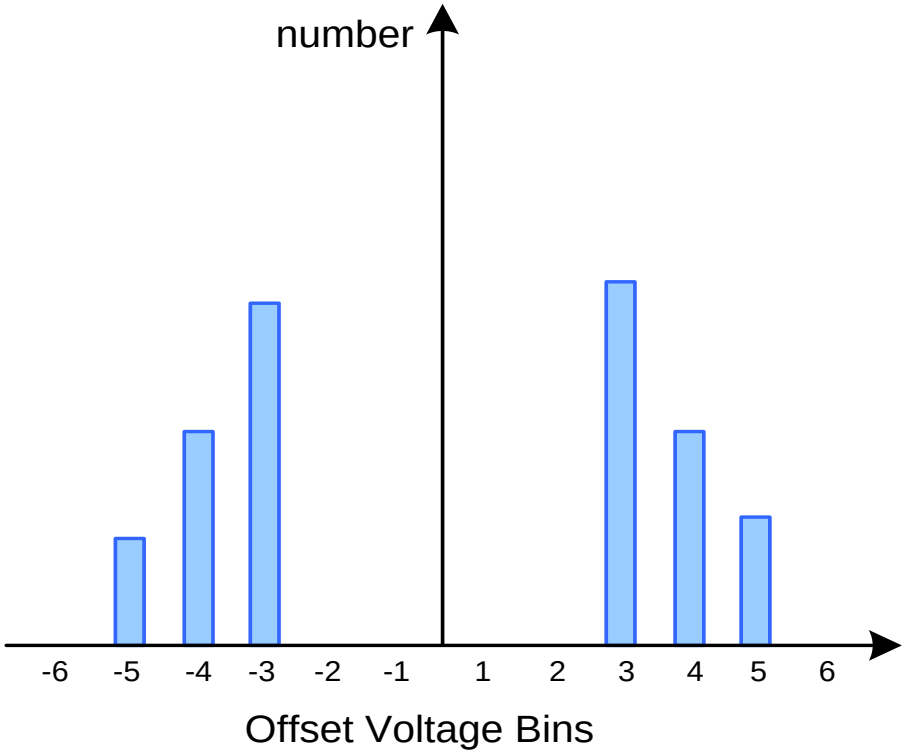
Offset Voltage Distribution



Typical histogram of offset voltage (binned) in shipped parts

Extreme offset parts have been sifted at test

Offset Voltage Distribution



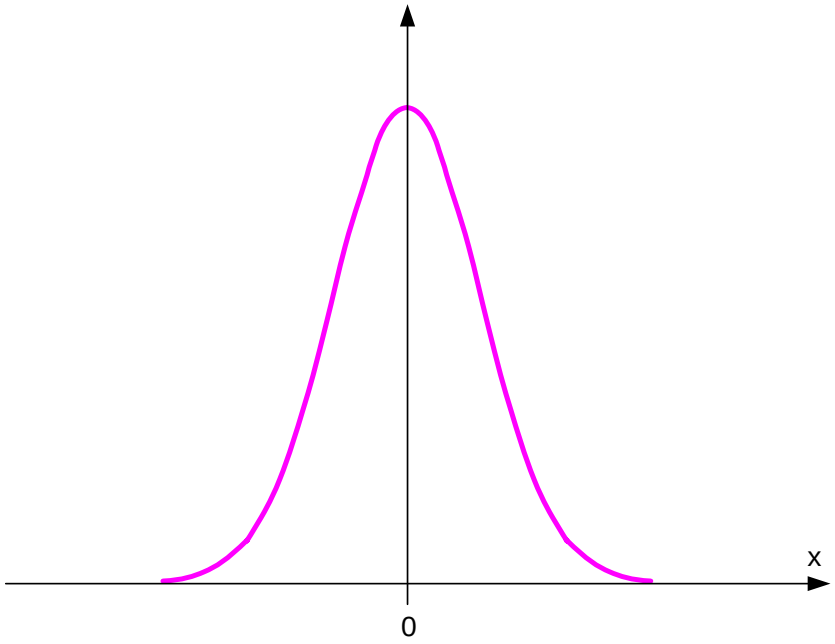
Typical histogram of offset voltage (binned) in shipped parts

Low-offset parts sometimes sold at a premium

Extreme offset parts have been sifted at test

Offset Voltage Distribution

Pdf of zero-mean Gaussian distribution



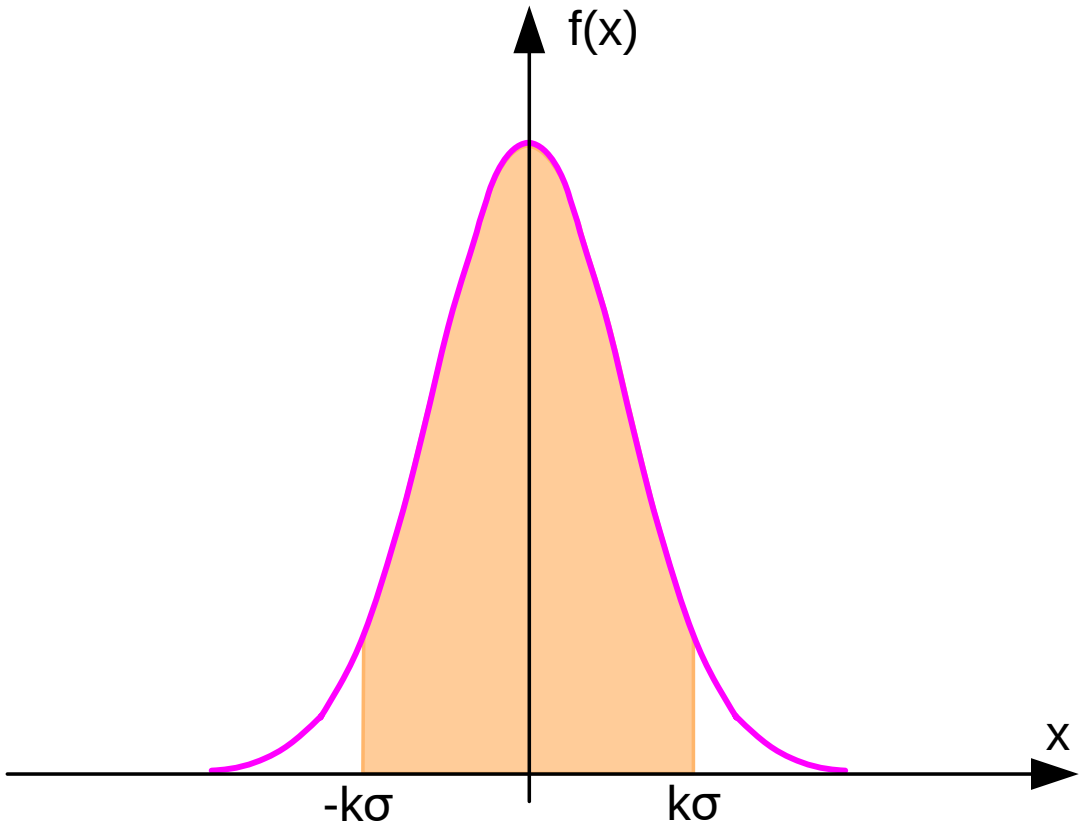
Characterized by its standard deviation σ or variance σ^2

Offset voltage often specified as the 1σ or 3σ value (though authors may neglect to indicate which)

For catalog parts, often specified as the worst-case value after sorted

Offset Voltage Distribution

Pdf of zero-mean Gaussian distribution



Percent between:	±σ	68.3%
	±2σ	95.5%
	±3σ	99.73%

Offset Voltage

TEXAS INSTRUMENTS

TL082 Wide Bandwidth Dual JFET Input Operational Amplifier

Check for Samples: TL082-N

FEATURES

- **Internally Trimmed Offset Voltage: 15 mV**
- **Low Input Bias Current: 50 pA**
- **Low Input Noise Voltage: 16nV/√Hz**
- **Low Input Noise Current: 0.01 pA/√Hz**
- **Wide Gain Bandwidth: 4 MHz**
- **High Slew Rate: 13 V/µs**
- **Low Supply Current: 3.6 mA**
- **High Input Impedance: $10^{12}\Omega$**
- **Low Total Harmonic Distortion: ≤0.02%**
- **Low 1/f Noise Corner: 50 Hz**
- **Fast Settling Time to 0.01%: 2 µs**

DESCRIPTION

These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL082 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and most LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low

DC Electrical Characteristics (1)

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C		5	15	mV
		Over Temperature			20	mV

Sifted at test is $|V_{OFF}|>15mV$

Guess 3σ value of trimmed but non-culled population is 15 mV

Offset Voltage

LM741 Operational Amplifier

1 Features

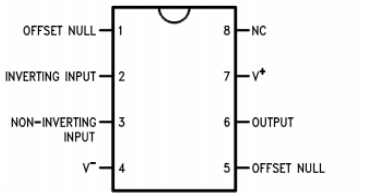
- Overload Protection on the Input and Output
- No Latch-Up When the Common-Mode Range is Exceeded

2 Applications

3 Description

The LM741 series are general-purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439, and 748 in most applications.

NAB Package
8-Pin CDIP or PDIP
Top View



6.5 Electrical Characteristics, LM741 (1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input offset voltage	$R_S \le 10\ k\Omega$	$T_A = 25°C$		1	5	mV
		$T_{AMIN} \le T_A \le T_{AMAX}$			6	mV
Input offset voltage adjustment range	$T_A = 25°C$, $V_S = \pm 20\ V$			±15		mV

Offset Voltage

FAIRCHILD SEMICONDUCTOR®

www.fairchildsemi.com

LM741

Single Operational Amplifier

Features

- Short circuit protection
- Excellent temperature stability
- Internal frequency compensation
- High Input voltage range
- Null of offset

Description

The LM741 series are general purpose operational amplifiers. It is intended for a wide range of analog applications. The high gain and wide range of operating voltage provide superior performance in intergrator, summing amplifier, and general feedback applications.

Electrical Characteristics

(V_{CC} = 15V, V_{EE} = - 15V. T_A = 25 °C, unless otherwise specified)

Parameter	Symbol	Conditions	LM741C/LM741I			Unit
			Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	R_S≤10KΩ	-	2.0	6.0	mV
		R_S≤50Ω	-	-	-	
Input Offset Voltage Adjustment Range	$V_{IO(R)}$	V_{CC} = ±20V	-	±15	-	mV
Input Offset Current	I_{IO}	-	-	20	200	nA
Input Bias Current	I_{BIAS}	-	-	80	500	nA

Offset Voltage

National Semiconductor

November 1994

LM741 Operational Amplifier

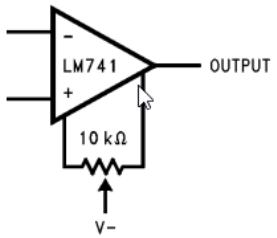
General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the co ceeded, as well as freedom from

The LM741C/LM741E are identi except that the LM741C/LM741 guaranteed over a 0°C to +70 stead of −55°C to +125°C.

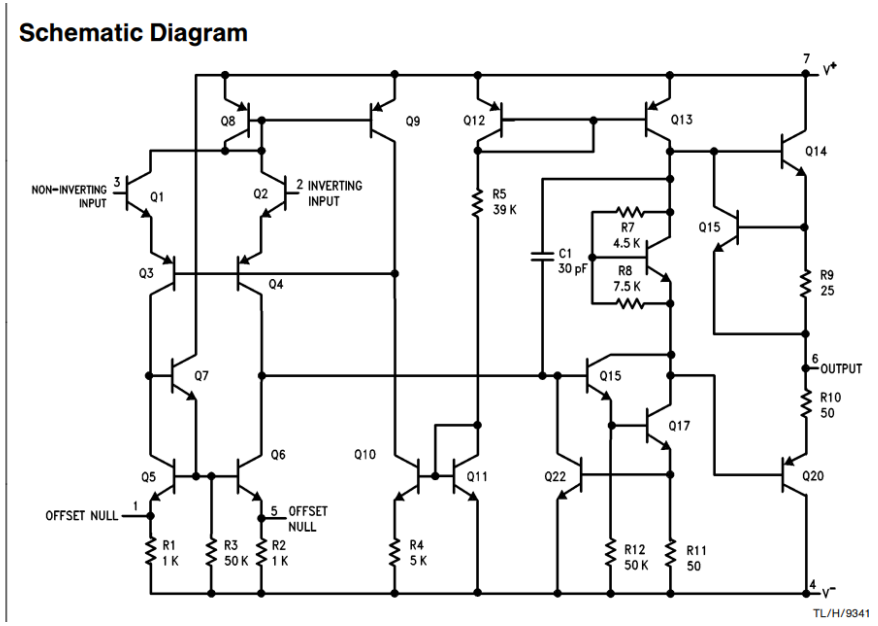
Offset Nulling Circuit



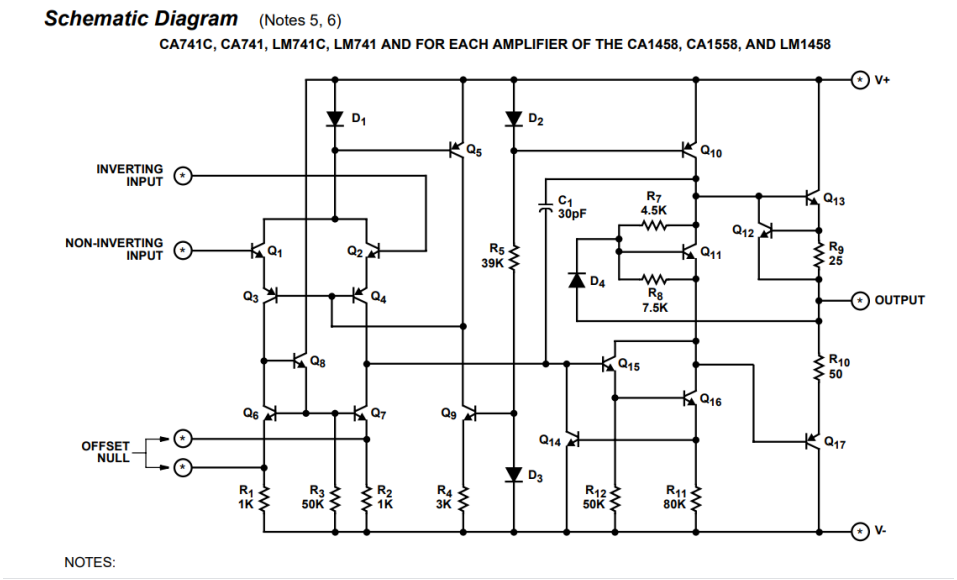
Electrical Characteristics (Note 3)

Parameter	Conditions	LM741A/LM741E			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$ $R_S \le 10\ k\Omega$ $R_S \le 50\Omega$		 0.8	 3.0		1.0	5.0		2.0	6.0	mV mV
	$T_{AMIN} \le T_A \le T_{AMAX}$ $R_S \le 50\Omega$ $R_S \le 10\ k\Omega$			4.0			 6.0			 7.5	mV mV
Average Input Offset Voltage Drift				15							μV/°C

Offset Voltage



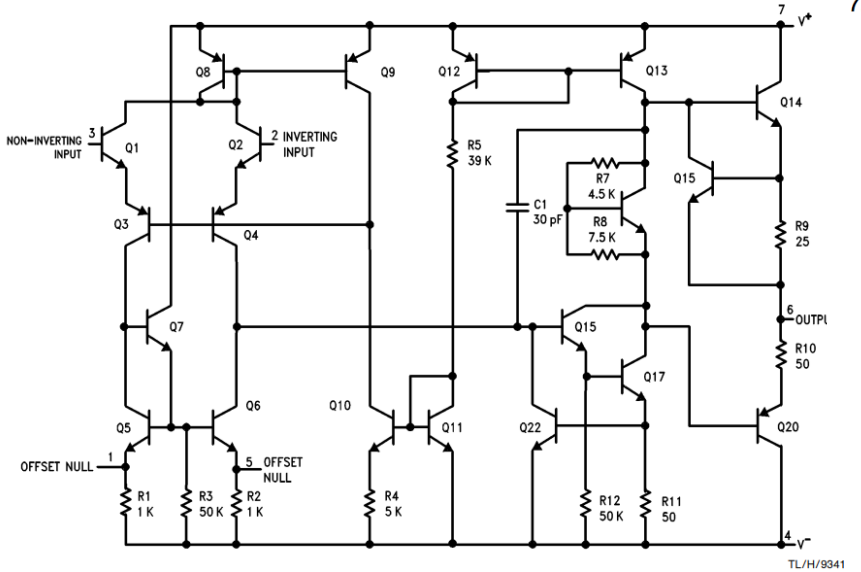
National



Intersil

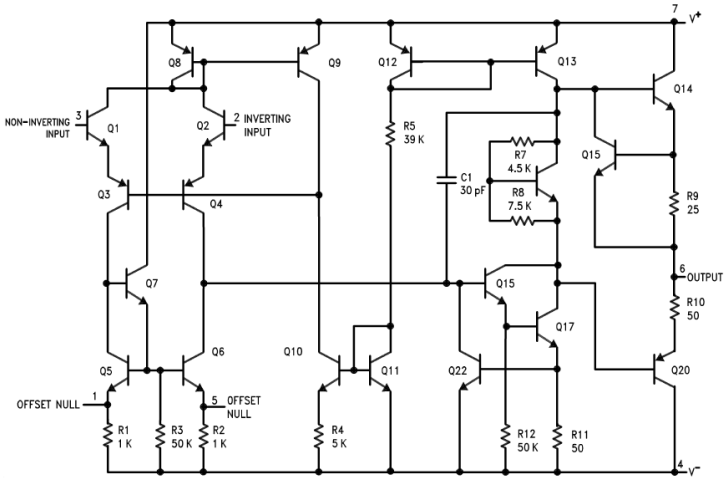
Offset Voltage

Schematic Diagram



National

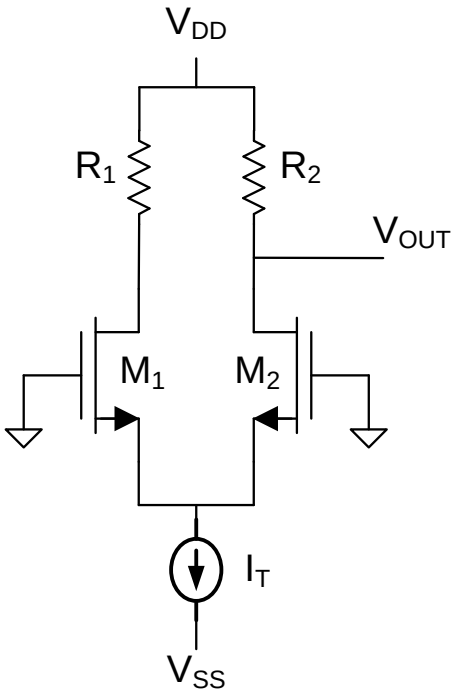
7.2 Functional Block Diagram



Texas Instruments

Source of Random Offset Voltages

Consider as an example:



Ideally $R_1=R_2=R$, M_1 and M_2 are matched

$$V_{OUT} = V_{DD} - \left(\frac{I_T}{2}\right)R$$

Assume this is the desired output voltage

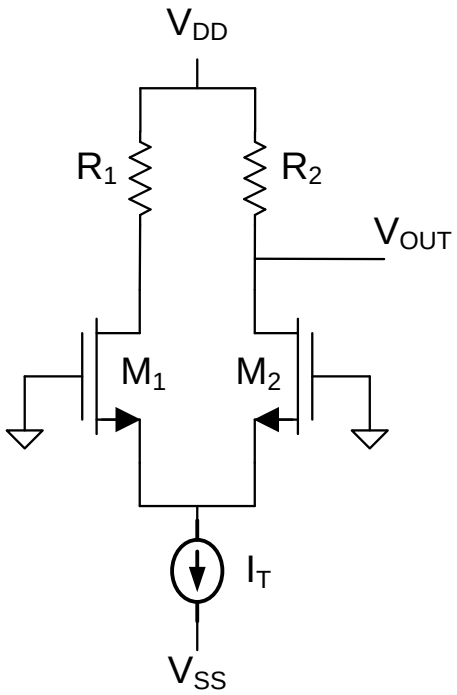
Source of Random Offset Voltages

Consider as an example:

Ideally

$R_1=R_2=R$

M_1 and M_2 matched



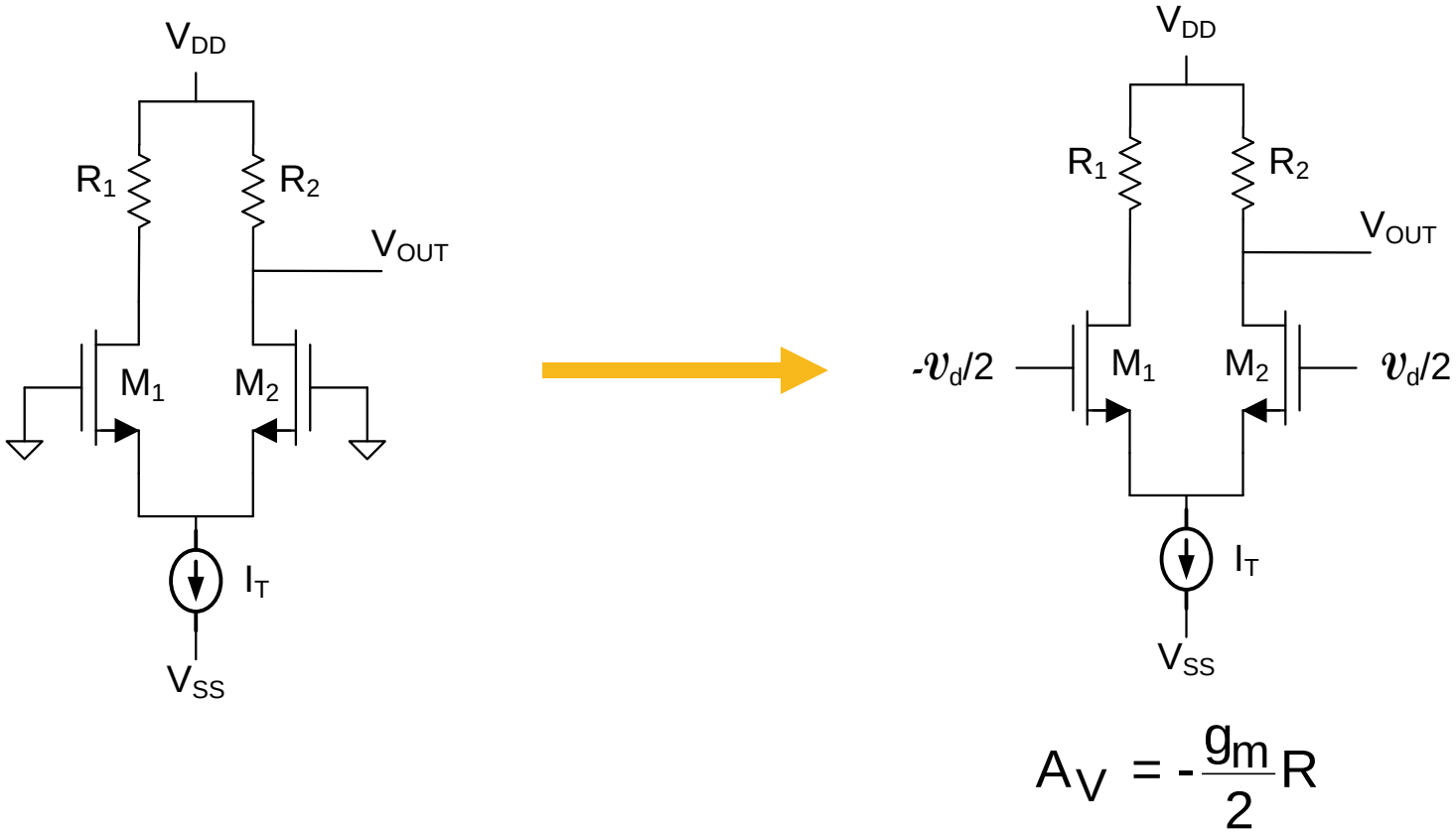
If everything ideal except $R_2=R+\Delta R$ (actually there will be mismatches between M_1 and M_2 also)

$$V_{OUT} = V_{DD} - \left(\frac{I_T}{2}\right)[R+\Delta R]$$

$$\Delta V_{OUT} = -\left(\frac{I_T}{2}\right)\Delta R$$

Source of Random Offset Voltages

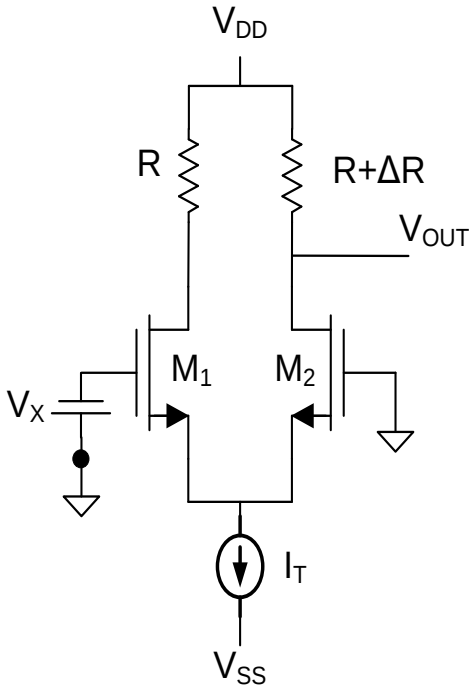
Consider as an example:



$$A_V = -\frac{g_m}{2}R$$

Source of Random Offset Voltages

Determine the offset voltage – i.e. value of V_X needed to obtain desired output



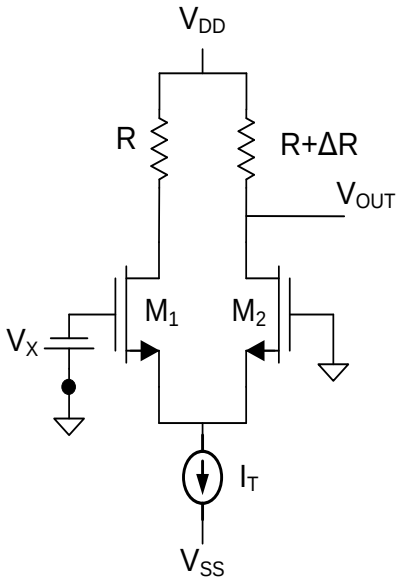
$$A_V = -\frac{g_m}{2}R$$

$$V_{OUT} = \left[V_{DD} - \left(\frac{I_T}{2}\right)R \right] - \left(\frac{I_T}{2}\right)\Delta R - A_V V_X$$

$$V_X = \frac{-1}{A_V}\left(\frac{I_T}{2}\right)\Delta R$$

Source of Random Offset Voltages

Determine the offset voltage – i.e. value of V_X needed to obtain desired output



$$A_V = -\frac{g_m}{2}R$$

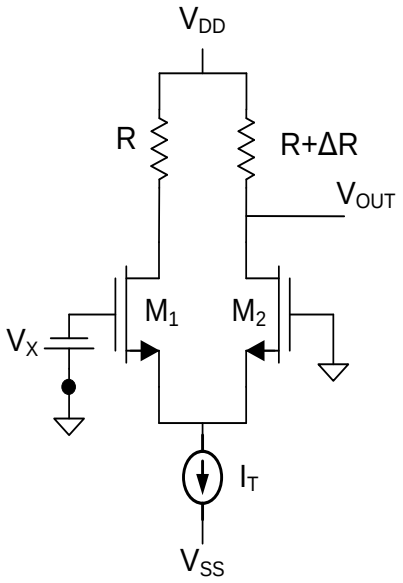
$$V_X = \frac{-1}{A_V}\left(\frac{I_T}{2}\right)\Delta R$$

$$V_X = \frac{2}{g_m R}\left(\frac{I_T}{2}\right)\Delta R = \left(\frac{I_T}{g_m}\right)\frac{\Delta R}{R} = \left(\frac{I_T}{I_T/V_{EB}}\right)\frac{\Delta R}{R} = V_{EB}\frac{\Delta R}{R}$$

$$V_X = V_{EB}\frac{\Delta R}{R}$$

Source of Random Offset Voltages

Determine the offset voltage – i.e. value of V_X needed to obtain desired output



$$A_V = -\frac{g_m}{2}R$$

$$V_X = V_{EB}\frac{\Delta R}{R}$$

What can the designer do to reduce the offset voltage if the resistor value and statistics are fixed?

Reduce V_{EB}

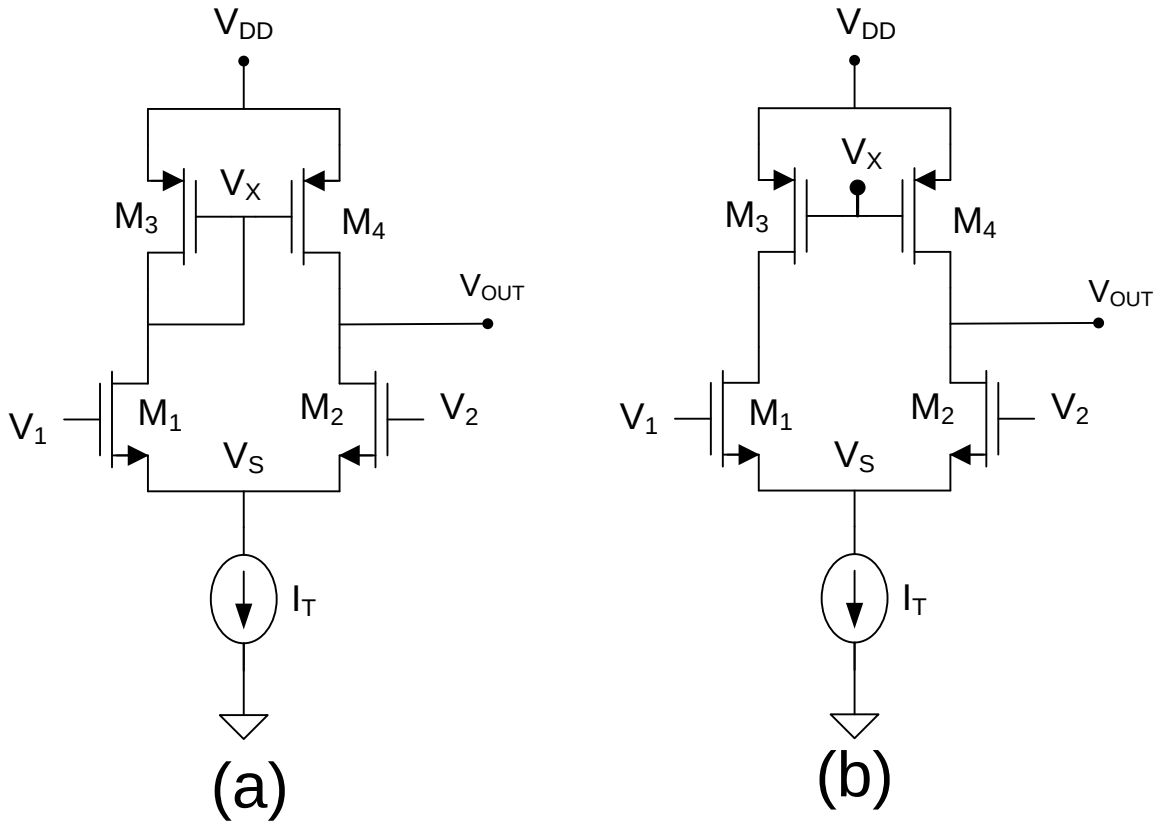
Will that affect the voltage gain?

$$A_V = -\frac{g_m}{2}R = \frac{2\frac{I_T}{2V_{EB}}}{2}R = \frac{1}{2V_{EB}}I_T R$$

Not if I_T is reduced by the same amount but that will affect signal swing and GB

Source of Random Offset Voltages

The random offset voltage is almost entirely that of the input stage in most op amps



Random Offset Voltage

- Due to random variations in process parameters and device dimensions
- Random offset is actually a random variable at the design level but deterministic after fabrication in any specific device
- Distribution naturally nearly Gaussian (could be un-naturally manipulated)

  Has zero mean

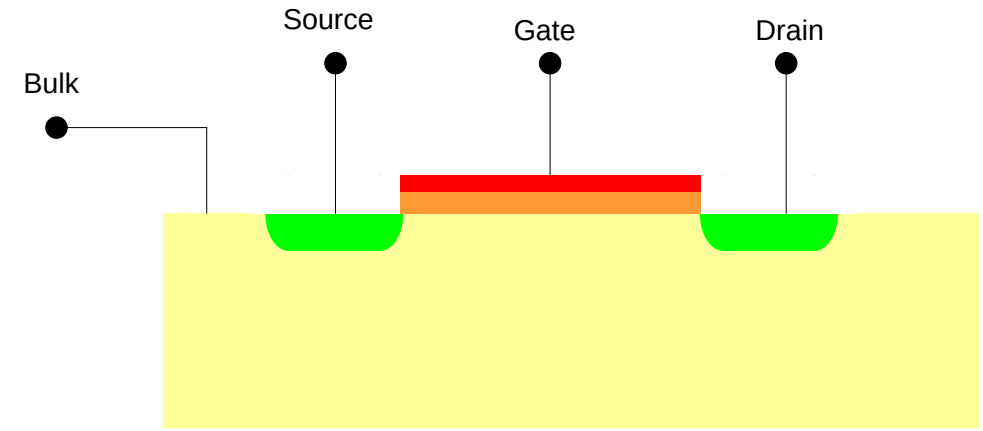
  Characterized by its standard deviation or variance

  Often strongly layout dependent

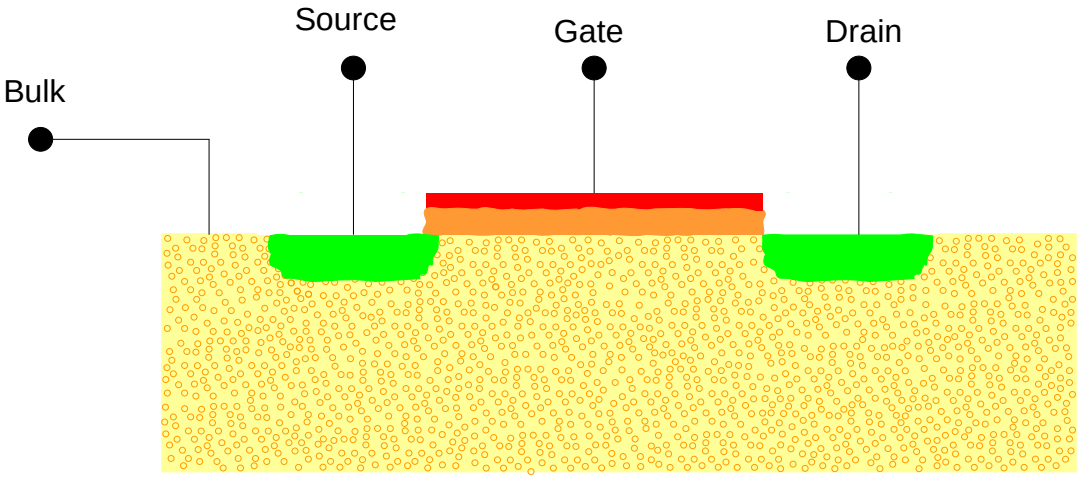
  Due to both local random variations and correlated gradient effects

  - Will consider both effects separately
  - Gradient effects usually dominate if not managed
  - Good methods exist for driving gradient effects to small levels

Offset Voltages due to Local Random Variations



n-channel MOSFET



n-channel MOSFET

Impurities vary randomly with position as do edges of gate, oxide and diffusions

Model and design parameters vary throughout channel and thus the corresponding equivalent lumped model parameters will vary from device to device

Model Parameter Variation

Define p to be a process parameter that varies with lateral position throughout the region defined by the channel of the transistor.

Almost Theorem:

If p(x,y) varies throughout a two-dimensional region, then

$$p_{EQ} = \frac{1}{A}\int_A p(x,y)\,dx\,dy$$

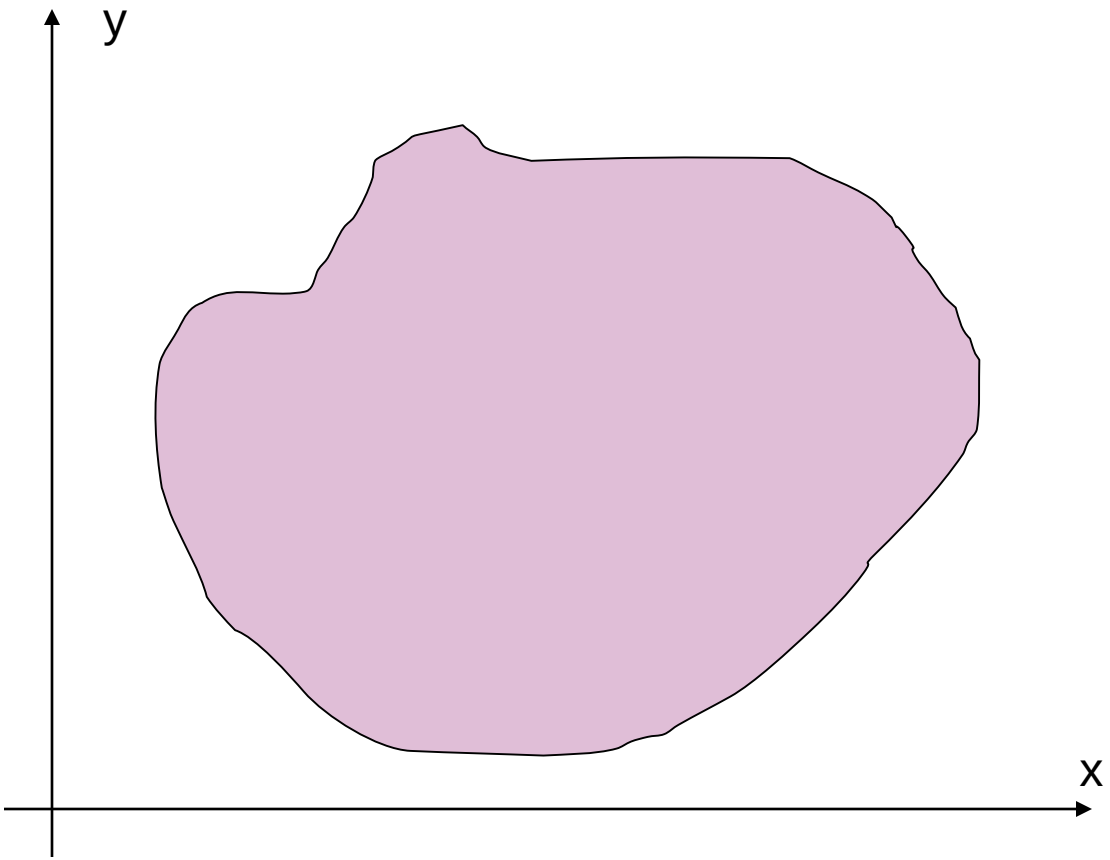
Parameters such at V_T, μ and C_{OX} vary throughout a two-dimensional region

Local random variations introduce a random component in device model parameters which are uncorrelated but for ideally matched devices they are identically distributed

e.g. $V_{TEQi}=V_{TN}+V_{TR\,i}$

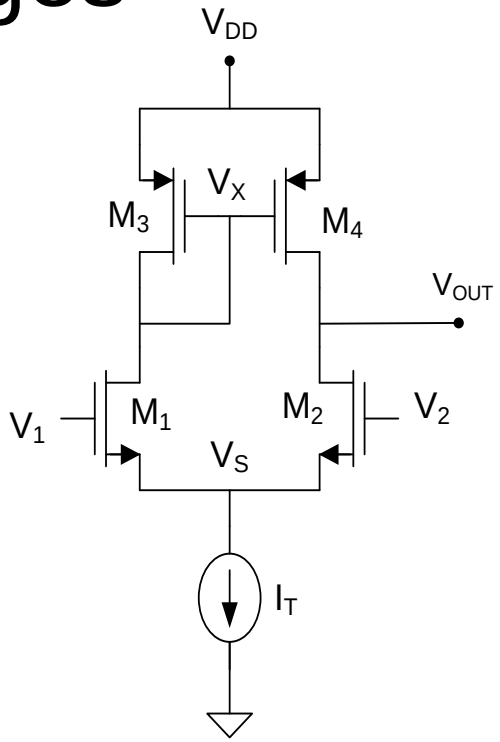
V_{TRi} and V_{TRj} due to local random variations are uncorrelated for $i \neq j$ but if ideally matched they are identically distributed

Model Parameter Variation



$$p_{EQ} = \frac{1}{A}\int_{A} p(x,y)\,dx\,dy$$

Random Offset Voltages



The random offset associated with <u>local random variations</u> is due to missmatches in the four transistors, dominantly missmatches in the parameters {V_T, μ,C_{OX},W and L}

The relative missmatch effects become more pronounced as devices become smaller

$$V_{Ti}=V_{TN}+V_{TRi}$$

$$C_{OXi}=C_{OXN}+C_{OXRi}$$

$$\mu_i=\mu_N+\mu_{Ri}$$

$$W_i=W_N+W_{Ri}$$

$$L_i=L_N+L_{Ri}$$

Each design and model parameter is comprised of a nominal part and a random component

It will be assumed that the random parts of each model parameter are uncorrelated but if ideally matched are identically distributed

(actually some small correlation in “model” parameters but will neglect in this course)

Random Offset Voltages

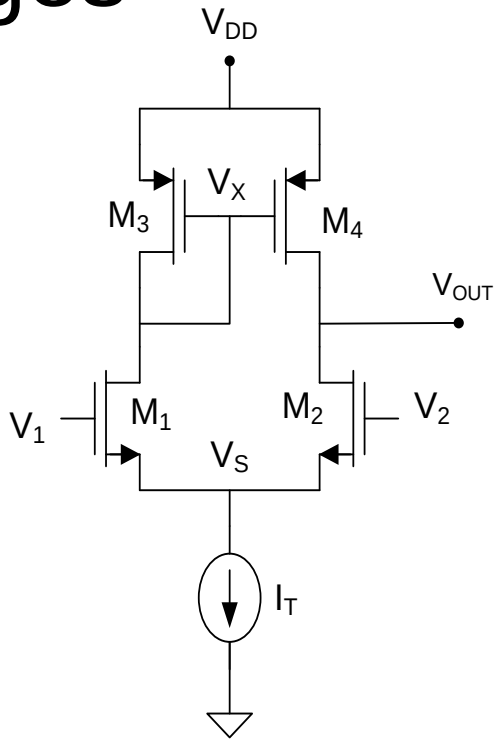
$$V_{Ti}=V_{TN}+V_{TRi}$$

$$C_{OXi}=C_{OXN}+C_{OXRi}$$

$$\mu_i=\mu_N+\mu_{Ri}$$

$$W_i=W_N+W_{Ri}$$

$$L_i=L_N+L_{Ri}$$



For each device, the device model is often expressed as

$$I_{Di} = \frac{(\mu_N+\mu_{Ri})(C_{OXN}+C_{OXRi})(W_N+W_{Ri})}{2(L_N+L_{Ri})}(V_{GSi}-(V_{TN}+V_{TRi}))^2(1+(\lambda_N+\lambda_{Ri})[V_{DS}])$$

Because of the random components of the parameters in every device, matching from the left-half circuit to the right half-circuit is not perfect

This mismatch introduces an offset voltage which is a random variable

Random Offset Voltages

From a straightforward but tedious analysis it follows that:

$$\sigma^2_{V_{OS}} = 2\left[\frac{A^2_{VTO\,n}}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2}A^2_{VTO\,p} + \frac{V^2_{EB\,n}}{4}\left(\frac{1}{W_n L_n}A^2_{\mu_n} + \frac{1}{W_p L_p}A^2_{\mu_p} + A^2_{COX}\left[\frac{1}{W_n L_n} + \frac{1}{W_p L_p}\right]\right.\right.$$
$$\left.\left. + 2A^2_L\left[\frac{1}{W_n L_n^2} + \frac{1}{W_p L_p^2}\right] + A^2_W\left[\frac{1}{L_n W_n^2} + \frac{1}{L_p W_p^2}\right]\right)\right]$$

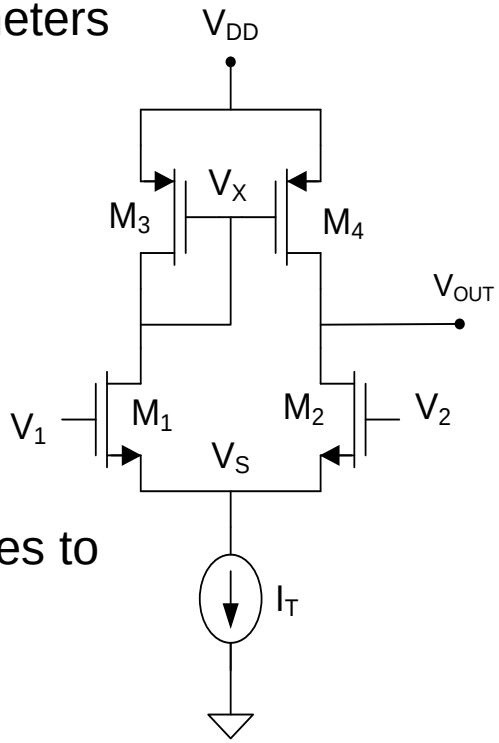
where the terms A_{VT0}, A_μ, A_{COX}, A_L, and A_W are process parameters

Typical values for matching model parameters:

$$A_{VT0} \cong \begin{cases} 21\text{mV}\bullet\mu & \text{(n-ch)} \\ 25\text{mV}\bullet\mu & \text{(p-ch)} \end{cases}$$

$$\sqrt{A_\mu^2 + A_{C_{OX}}^2} \cong \begin{cases} .016\mu & \text{(n-ch)} \\ .023\mu & \text{(p-ch)} \end{cases}$$

$$A_L = A_W \cong 0.017\mu^{3/2}$$



Usually the A_{VT0} terms are dominant, thus the variance simplifies to

$$\sigma^2_{V_{OS}} \cong 2\left[\frac{A^2_{VTO\,n}}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2}A^2_{VTO\,p}\right]$$

(Remember this is due to local random variations)

Random Offset Voltages

$$\sigma^2_{V_{OS}} \cong 2\left[\frac{A^2_{VTO\,n}}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2} A^2_{VTO\,p}\right]$$

This expression has somewhat peculiar coefficients. The first term on the right is dependent upon the reciprocal of the area of the n-channel device but the corresponding coefficient on the second term on the right appears to depend upon the dimensions of both the n-channel and p-channel devices. But this can be rewritten as

$$\sigma^2_{V_{OS}} \cong 2\left[\frac{A^2_{VTO\,n}}{W_n L_n} + \left(\frac{V_{EB\,n}}{V_{EB\,p}}\right)^2 \frac{A^2_{VTO\,p}}{W_p L_p}\right]$$

The dependence of the variance on the area of the n-channel and p-channel devices is more apparent when written in this form.

Random Offset Voltages

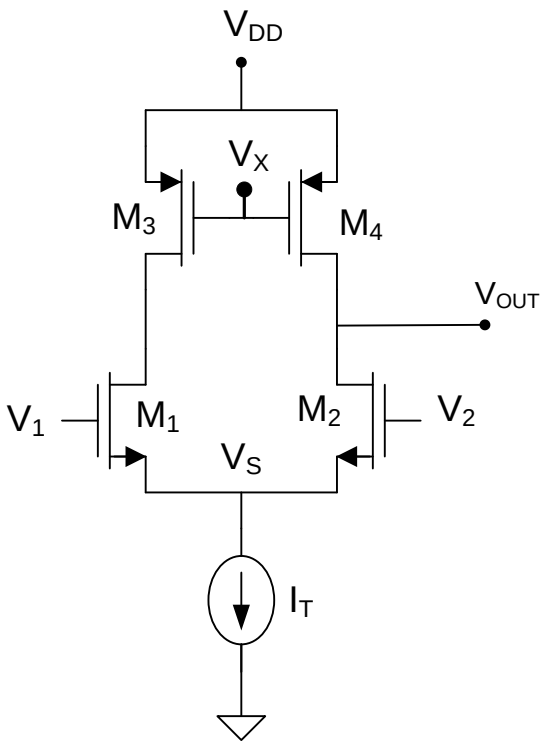
Correspondingly:

$$\sigma^2_{V_{OS}} = 2\left[\frac{A^2_{VTOn}}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2}A^2_{VTOp} + \frac{V^2_{EBn}}{4}\left(\begin{array}{l}\frac{1}{W_n L_n}A^2_{\mu_n} + \frac{1}{W_p L_p}A^2_{\mu_p} + A^2_{COX}\left[\frac{1}{W_n L_n} + \frac{1}{W_p L_p}\right] \\ + 2A^2_L\left[\frac{1}{W_n L_n^2} + \frac{1}{W_p L_p^2}\right] + A^2_w\left[\frac{1}{L_n W_n^2} + \frac{1}{L_p W_p^2}\right]\end{array}\right)\right]$$

which again simplifies to

$$\sigma^2_{V_{OS}} \cong 2\left[\frac{A^2_{VTO\,n}}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2}A^2_{VTO\,p}\right]$$

Note these offset voltage expressions are identical!

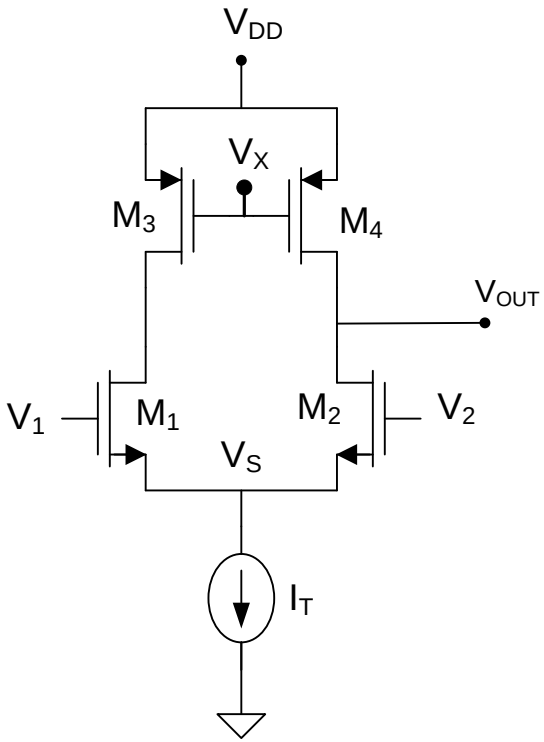


Random Offset Voltages

Example: Determine the 3σ value of the input offset voltage for The MOS differential amplifier if

a) M_1 and M_3 are minimum-sized and

b) the area of M_1 and M_3 are 100 times minimum size



$$\sigma^2_{V_{OS}} \cong 2\left[\frac{A^2_{VTO\,n}}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2} A^2_{VTO\,p}\right]$$

$$\sigma^2_{V_{OS}} \cong \frac{2}{W_n L_n}\left[A^2_{VTO\,n} + \frac{\mu_p}{\mu_n} A^2_{VTO\,p}\right]$$

a)

$$\sigma^2_{V_{OS}} \cong \frac{2}{(0.5\mu)^2}\left[.021^2 + \frac{1}{3}.025^2\right]$$

$$\sigma_{V_{OS}} \cong 72\text{mV}$$

$$3\,\sigma_{V_{OS}} \cong 216\text{mV}$$

Note this is a very large offset voltage !

Random Offset Voltages

Example: Determine the 3σ value of the input offset voltage for the MOS differential amplifier due to local random variations if:

a) M_1 and M_3 are minimum-sized and

b) the area of M_1 and M_3 are 100 times minimum size

$$\sigma^2_{V_{OS}} \cong 2\left[\frac{A^2_{VTO\,n}}{W_n L_n} + \frac{\mu_p}{\mu_n}\frac{L_n}{W_n L_p^2} A^2_{VTO\,p}\right]$$

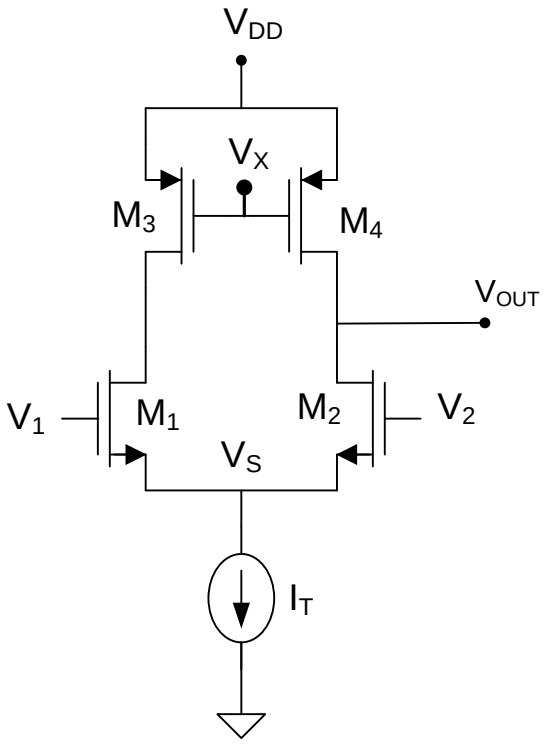
$$\sigma^2_{V_{OS}} \cong \frac{2}{W_n L_n}\left[A^2_{VTO\,n} + \frac{\mu_p}{\mu_n} A^2_{VTO\,p}\right]$$

b)

$$\sigma^2_{V_{OS}} \cong \frac{2}{100(0.5\mu)^2}\left[.021^2 + \frac{1}{3}.025^2\right]$$

$$\sigma_{V_{OS}} \cong 7.2\text{mV}$$

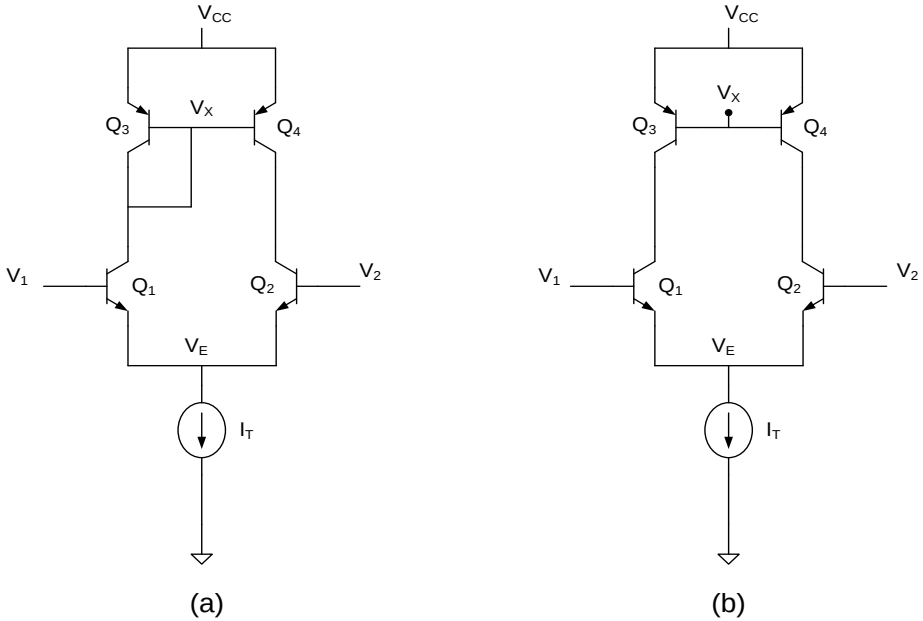
$$3\,\sigma_{V_{OS}} \cong 21.6\text{mV}$$



Note this is much lower but still a large offset voltage !

The area of M_1 and M_3 need to be very large to achieve a low offset voltage

Random Offset Voltages



It can be shown that

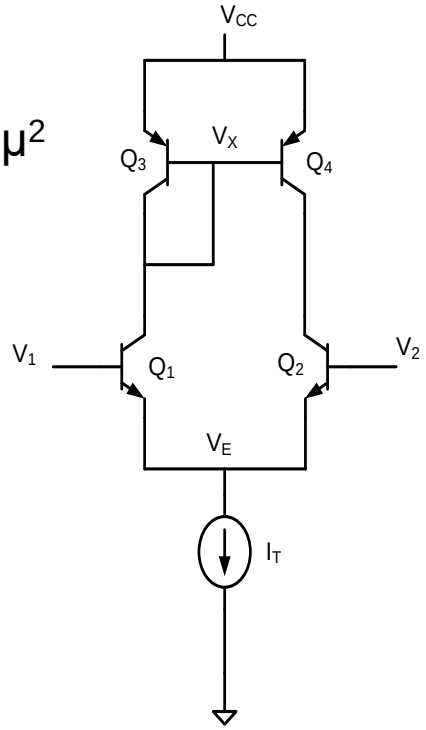
$$\sigma_{V_{OS}}^2 \cong 2V_t^2\left[\frac{A_{Jn}^2}{A_{En}} + \frac{A_{Jp}^2}{A_{Ep}}\right]$$

where very approximately

$$A_{Jn} = A_{Jp} = 0.1\mu$$

Random Offset Voltages

Example: Determine the 3σ value of the offset voltage of a the bipolar input stage due to local random variations if $A_{E1}=A_{E3}=10\mu^2$



$$\sigma^2_{V_{OS}} \cong 2V_t^2\left[\frac{A^2_{Jn}}{A_{En}}+\frac{A^2_{Jp}}{A_{Ep}}\right]$$

$$\sigma_{V_{OS}} \cong \sqrt{2}V_t\, A_J \frac{\sqrt{2}}{\sqrt{A_E}}$$

$$\sigma_{V_{OS}} \cong 2 \bullet 25\text{mV} \bullet 0.1\mu \bullet \frac{1}{\sqrt{10\mu^2}} = 1.6\text{mV}$$

$$3\sigma_{V_{OS}} \cong 4.7\text{mV}$$

Note this value is much smaller than that for the MOS input structure !

Random Offset Voltages

Typical offset voltages:

MOS - 5mV to 50MV
BJT - 0.5mV to 5mV

These can be scaled with extreme device dimensions

Often more practical to include offset-compensation circuitry

Random Offset Voltage

- Due to random variations in process parameters and device dimensions
- Random offset is actually a random variable at the design level but deterministic after fabrication in any specific device
- Distribution naturally nearly Gaussian (could be un-naturally manipulated)

  Has zero mean

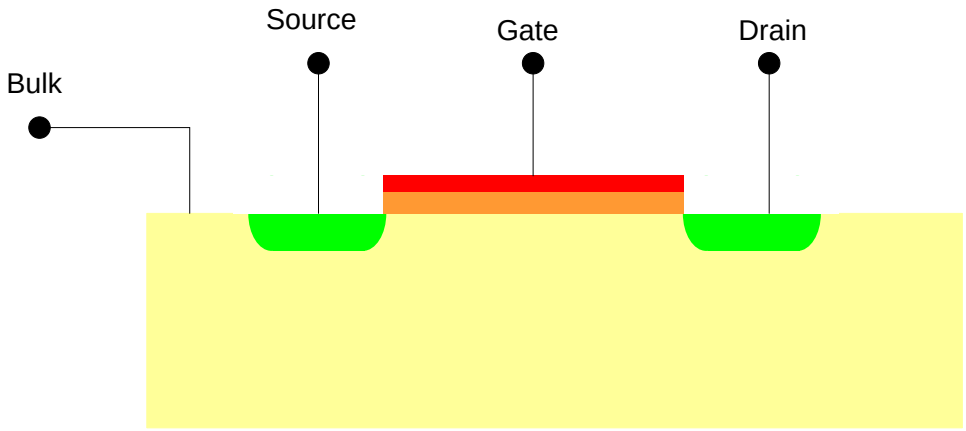
  Characterized by its standard deviation or variance

  Often strongly layout dependent

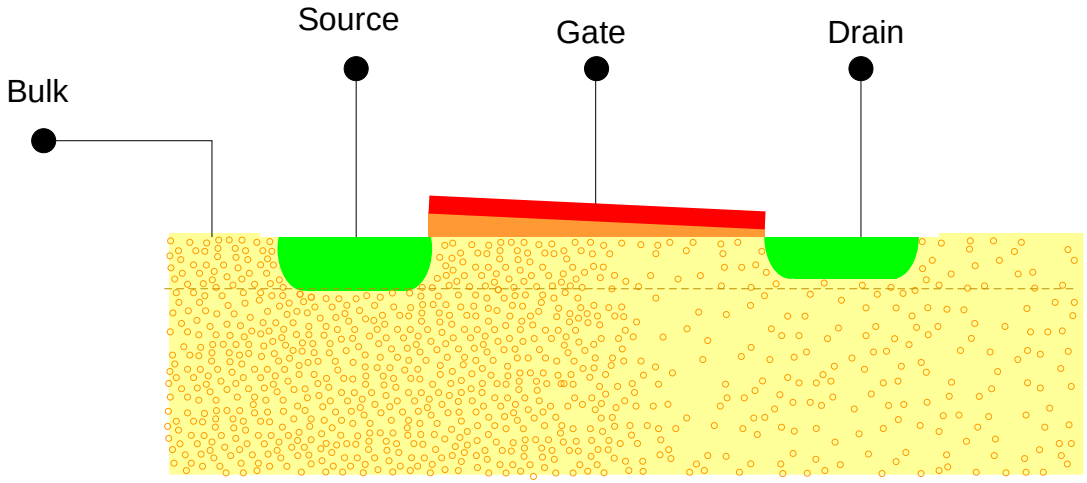
  Due to both local random variations and correlated gradient effects

  - Will consider both effects separately
  - Gradient effects usually dominate if not managed
  - Good methods exist for driving gradient effects to small levels

Offset Voltages due to Gradients



n-channel MOSFET



n-channel MOSFET

Impurity density or layer thicknesses vary linearly through the channel

Model and design parameters vary throughout channel and thus the corresponding equivalent lumped model parameters will vary from device to device

Model Parameter Variation

Define p to be a process parameter that varies with lateral position throughout the region defined by the channel of the transistor.

Almost Theorem:

If p(x,y) varies throughout a two-dimensional region, then

$$p_{EQ} = \frac{1}{A}\int_A p(x,y)\,dx\,dy$$

Parameters such at V_T, μ and C_{OX} vary throughout a two-dimensional region

Gradients

~~Local random variations~~ introduce a random component in device model parameters which are ~~uncorrelated~~ correlated for neighborhood devices but for ideally matched devices they are identically distributed e.g. $V_{TEQi}=V_{TN}+V_{TR\,i}$

gradients correlated

V_{TRi} and V_{TRj} due to ~~local random variations~~ are ~~uncorrelated~~ for i≠j but if ideally matched they are identically distributed

Common Centroid Layouts

Define p to be a process parameter that varies linearly with lateral position throughout the region defined by the channel of the transistor.

Almost Theorem:

If p(x,y) varies linearly throughout a two-dimensional region, then

$$p_{EQ} = \frac{1}{A}\int_{A} p(x,y)\,dx\,dy$$

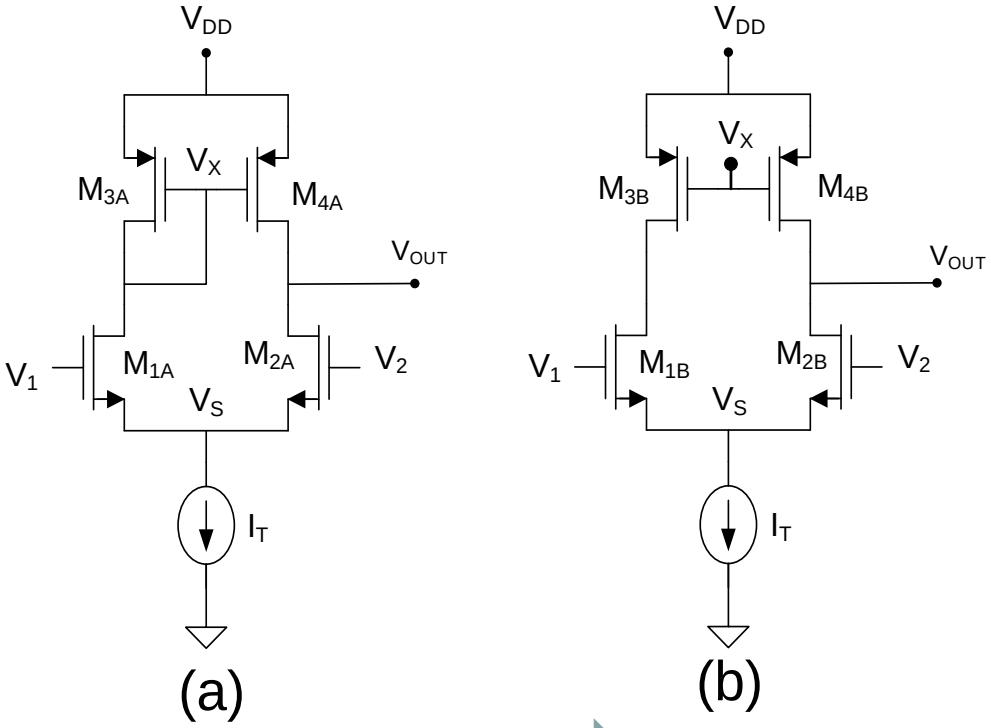
Gradient effects cause parameters such at V_T, μ and C_{OX} to vary approximately linearly throughout a two-dimensional region

The direction and magnitude of gradients are random variables but are correlated and identical for closely-placed devices

Source of Random Offset Voltages

The random offset voltage is almost entirely that of the input stage in most op amps

Assume schematic representative of placement of devices in layout



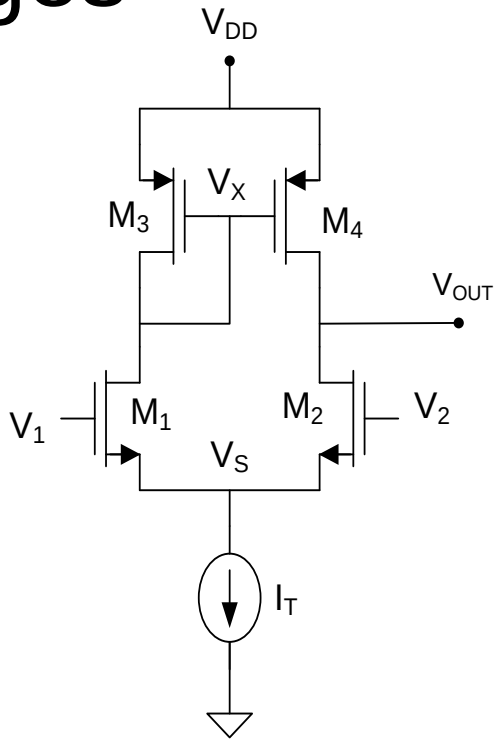
If threshold gradient in this direction and local random variations are neglected

$$V_{TH2A} = V_{TH1A} + \alpha d$$

α is the magnitude of the gradient

d is the distance between M_{1A} and M_{2A}

Random Offset Voltages



The random offset associated with local random variations is due to missmatches in the four transistors, dominantly missmatches in the parameters {V_T, μ,C_{OX},W and L}

Gradient effects and local random variations are both present and additive

$$V_{Ti}=V_{TN}+V_{TRi}+V_{TGi}$$

$$C_{OXi}=C_{OXN}+C_{OXRi}+C_{OXGi}$$

$$\mu_i=\mu_N+\mu_{Ri}+\mu_{Gi}$$

$$W_i=W_N+W_{ri}+W_{Gi}$$

$$L_i=L_N+L_{ri}+L_{Gi}$$

Each design and model parameter is comprised of a nominal part and a random component

The local random parts of each model parameter are uncorrelated but if ideally matched are identically distributed and the gradient parts for closely placed devices are correlated

Gradients are uncorrelated with local random variations

Recall:

Model Parameter Variations

Define p to be a process parameter that varies with lateral position throughout the region defined by the channel of the transistor.

Almost Theorem:

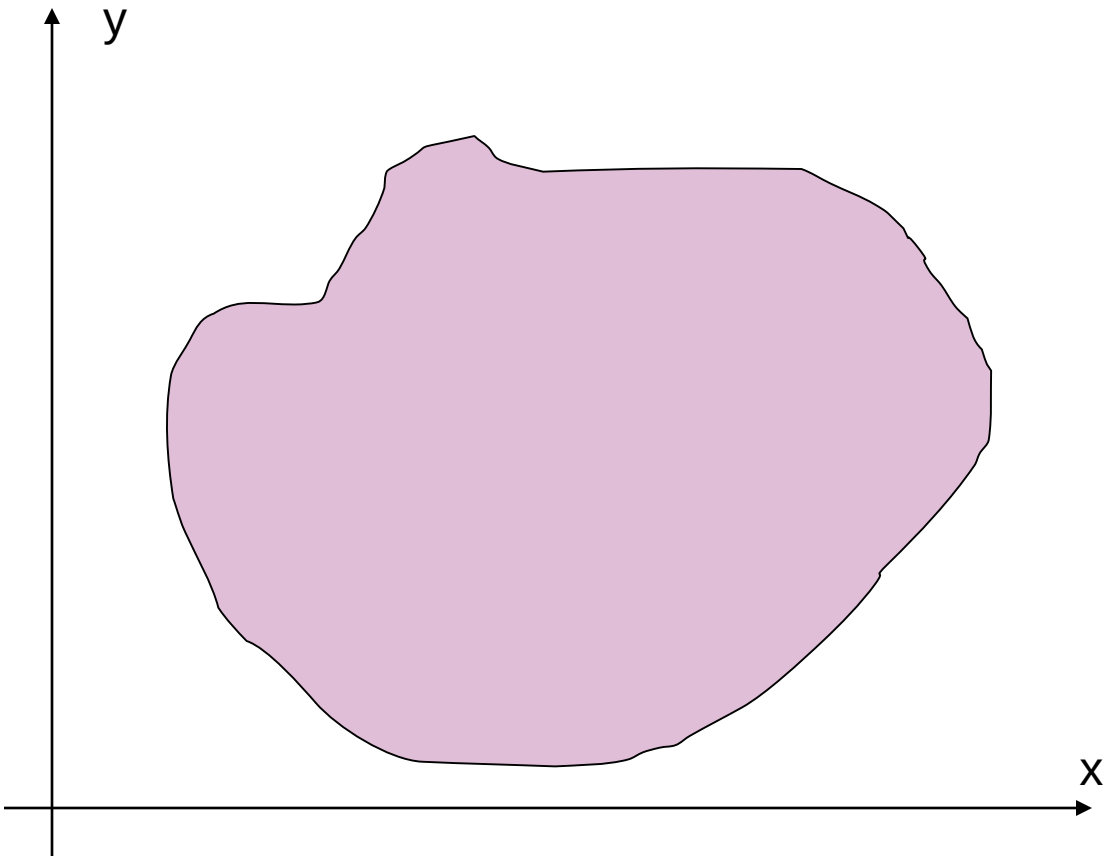
If p(x,y) varies throughout a two-dimensional region, then

$$p_{EQ} = \frac{1}{A}\int_{A} p(x,y)\,dx\,dy$$

Parameters such at V_T, μ and C_{OX} vary throughout a two-dimensional region

Recall:

Model Parameter Variations



$$p_{EQ} = \frac{1}{A}\int_{A} p(x,y)\,dx\,dy$$

Common Centroid Layouts

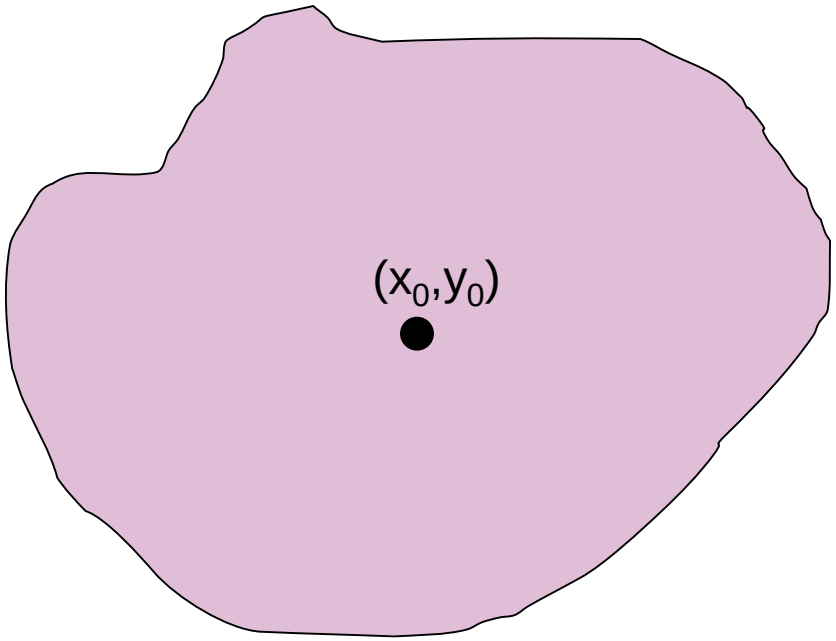
Almost Theorem:

If p(x,y) varies linearly throughout a two-dimensional region, then $p_{EQ}=p(x_0.y_0)$ where x_0,y_0 is the geometric centroid to the region.

If a parameter varies linearly throughout a two-dimensional region, it is said to have a linear gradient.

Many parameters have a dominantly linear gradient over rather small regions but large enough to encompass layouts where devices are ideally matched

Common Centroid Layouts



(x_0,y_0) is geometric centroid

$$p_{EQ} = \frac{1}{A}\int_A p(x,y)\,dx\,dy$$

If ρ(x,y) varies linearly in any direction, then the theorem states

$$p_{EQ} = \frac{1}{A}\int_A p(x,y)\,dx\,dy = p(x_0,y_0)$$

Common Centroid Layouts

Definition: A layout of two devices is termed a common-centroid layout if both devices have the same geometric centroid

Almost Theorem:

If p(x,y) varies linearly throughout a two-dimensional region, then if two devices have the same centroid, the lateral-variable parameters are matched !

Note: This is true independent of the magnitude and direction of the gradient!

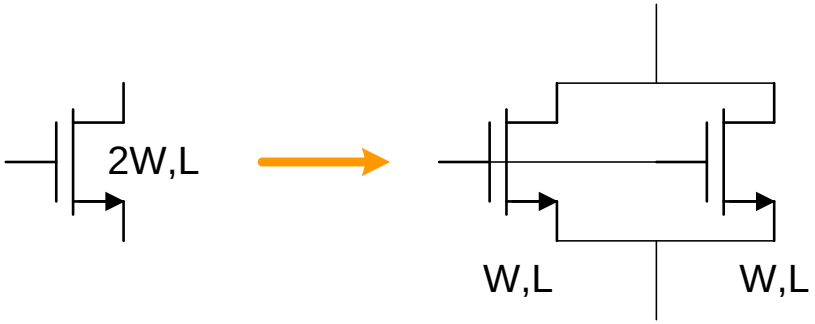
Almost Theorem:

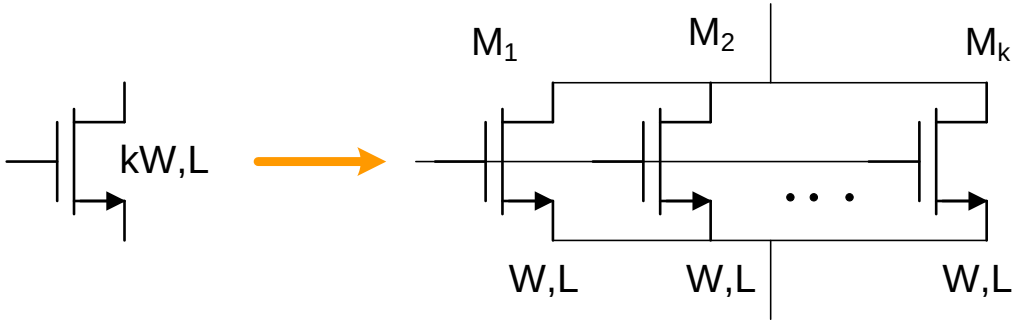
If a common-centroid layout is used for the matching-critical part of an operational amplifier, the lateral-variable parameters (e.g. V_{TH}, μ, C_{OX}) will introduce no offset voltage!

Common-centroid layouts almost always used for matching-critical components to eliminate linear gradients of critical parameters !

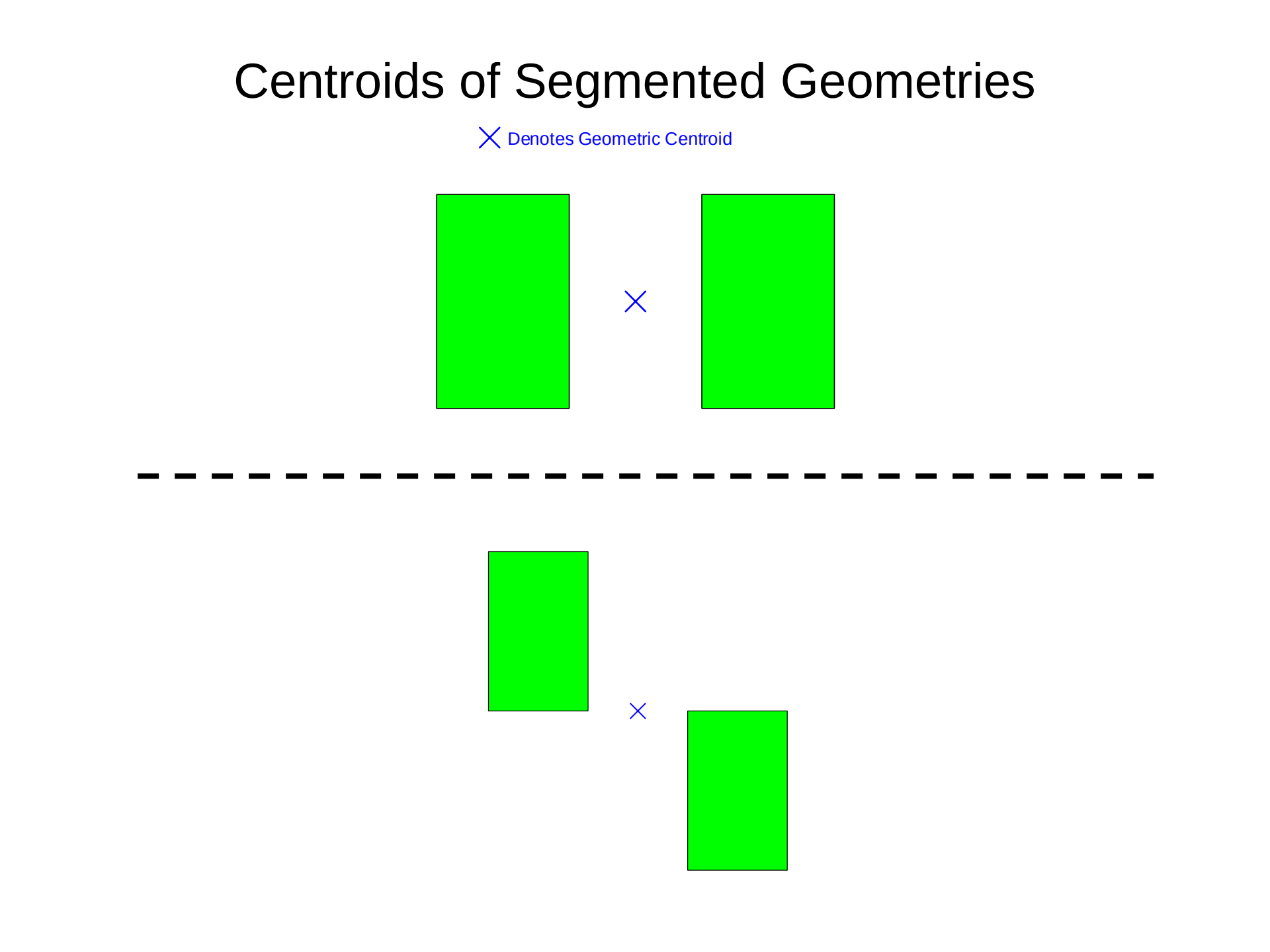
But local random variations will still affect matching even if gradient effects are eliminated

Recall parallel combinations of transistors equivalent to a single transistor of appropriate W,L

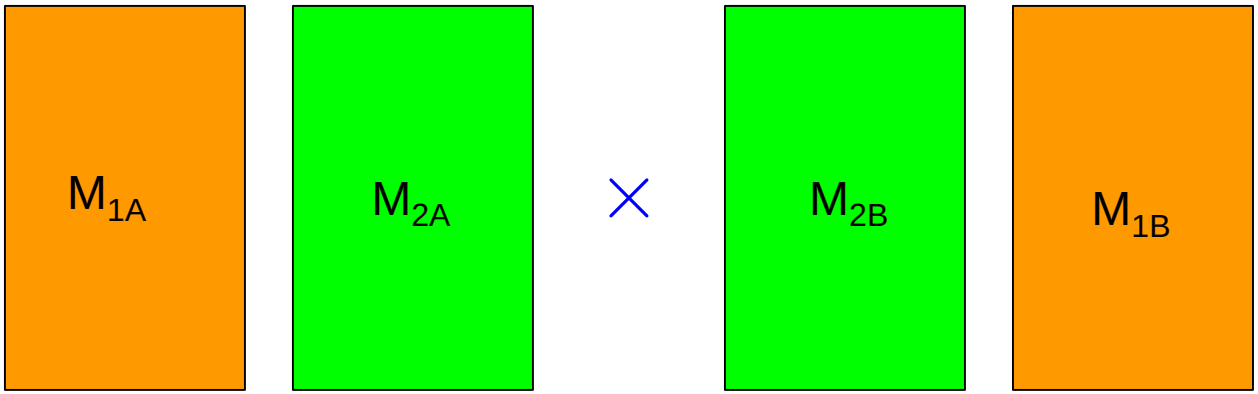


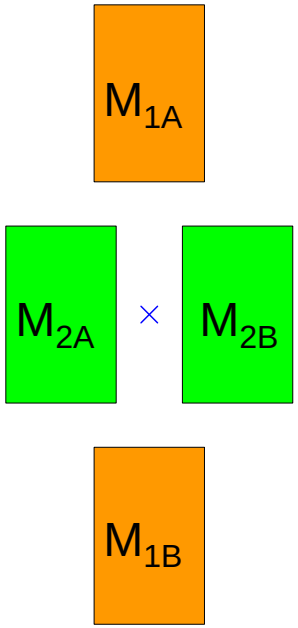


Centroids of Segmented Geometries



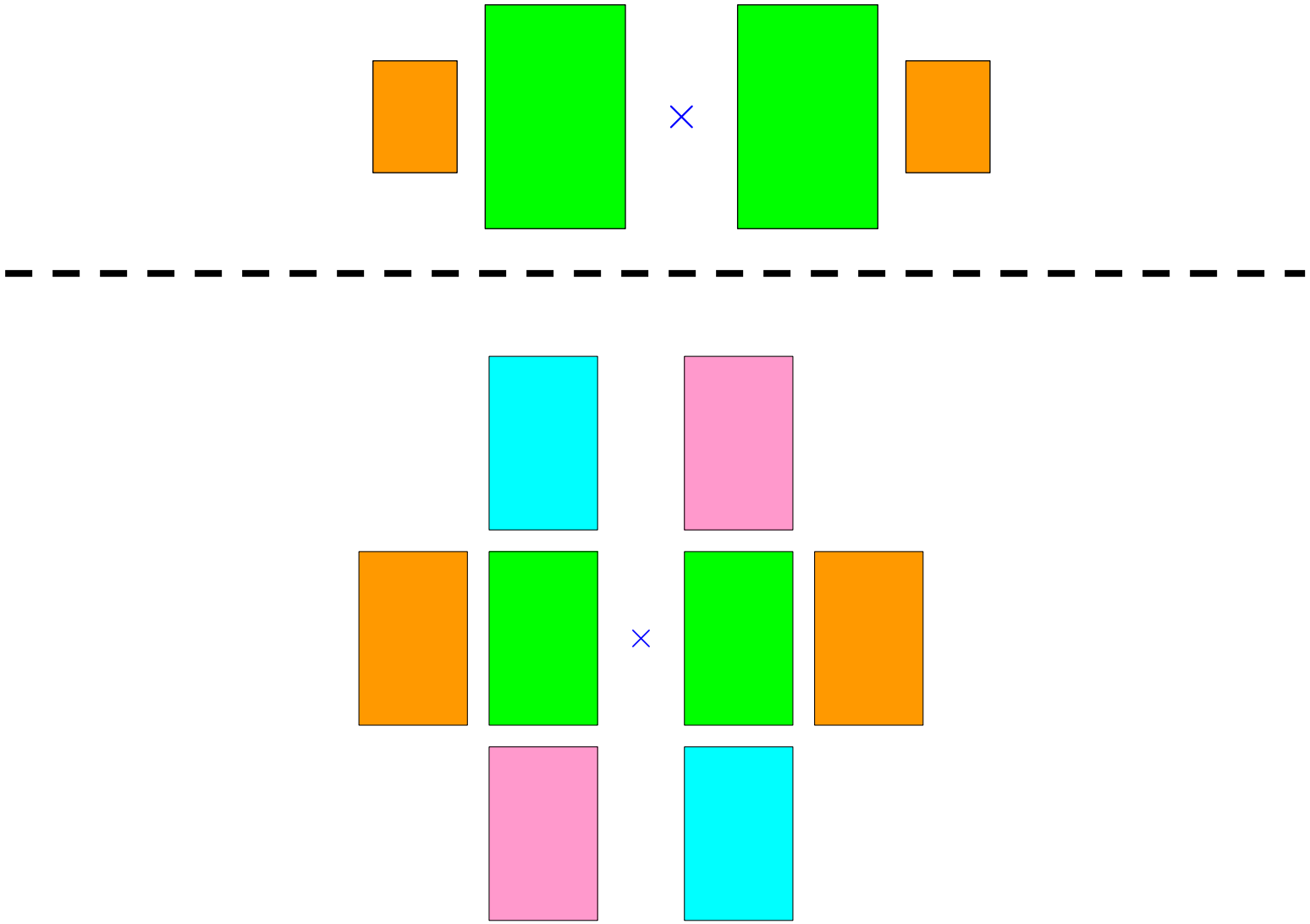
Common Centroid of Multiple Segmented Geometries



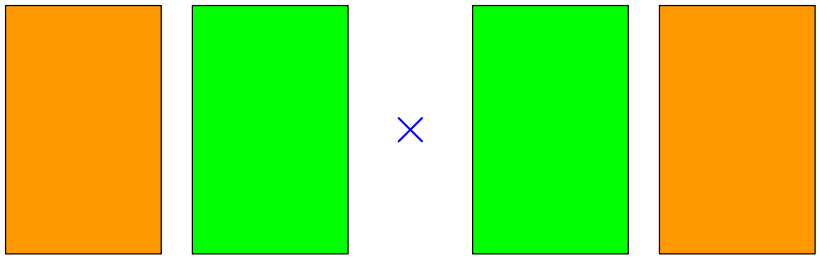


If these are layouts of gates of two transistors with two segments, M_1 and M_2 have common centroids. They are thus termed common-centroid layouts

Common Centroid of Multiple Segmented Geometries



Common Centroid Layouts



Common centroid layouts widely (almost always) used where matching of devices or components is critical because these layouts will cancel all first-order gradient effects

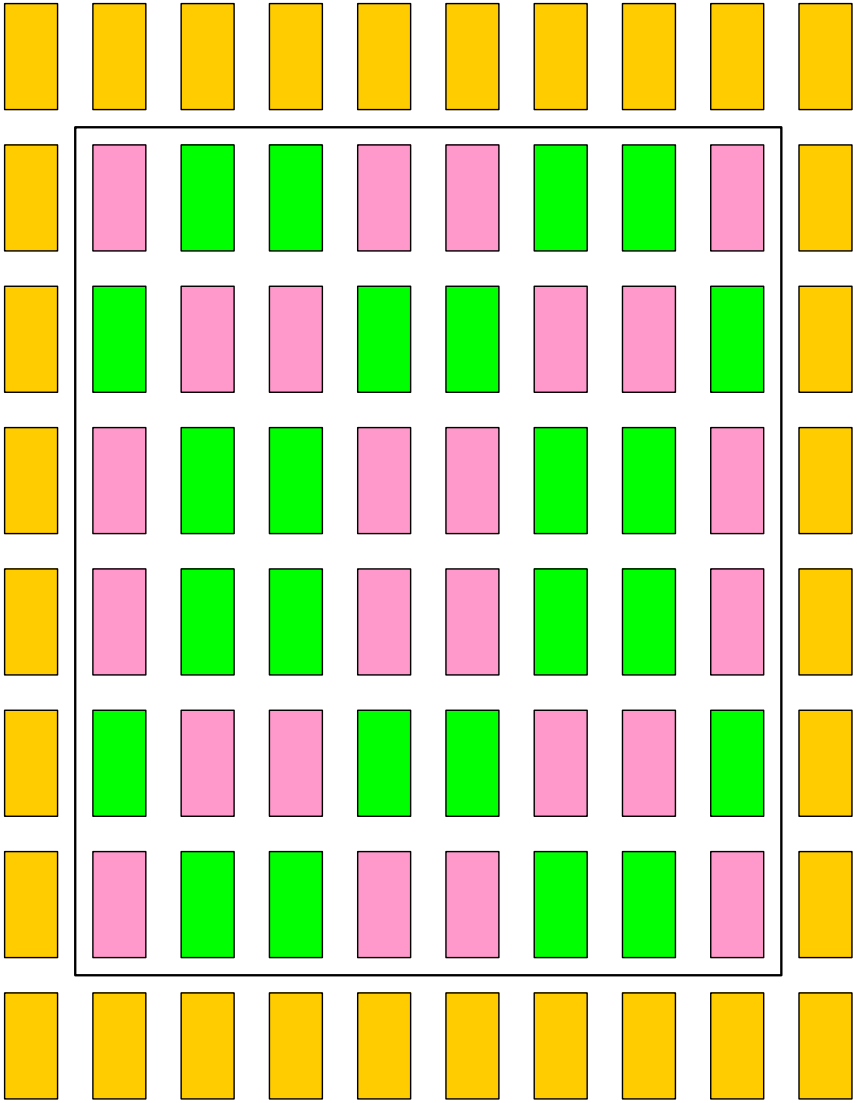
Applies to resistors, capacitors, transistors and other components

Always orient all devices in the same way

Keep common centroid for interconnects, diffusions, and all features

Often dummy devices placed on periphery to improve matching !

Common Centroid Layout Surrounded by Dummy Devices



Stay Safe and Stay Healthy !

End of Lecture 22